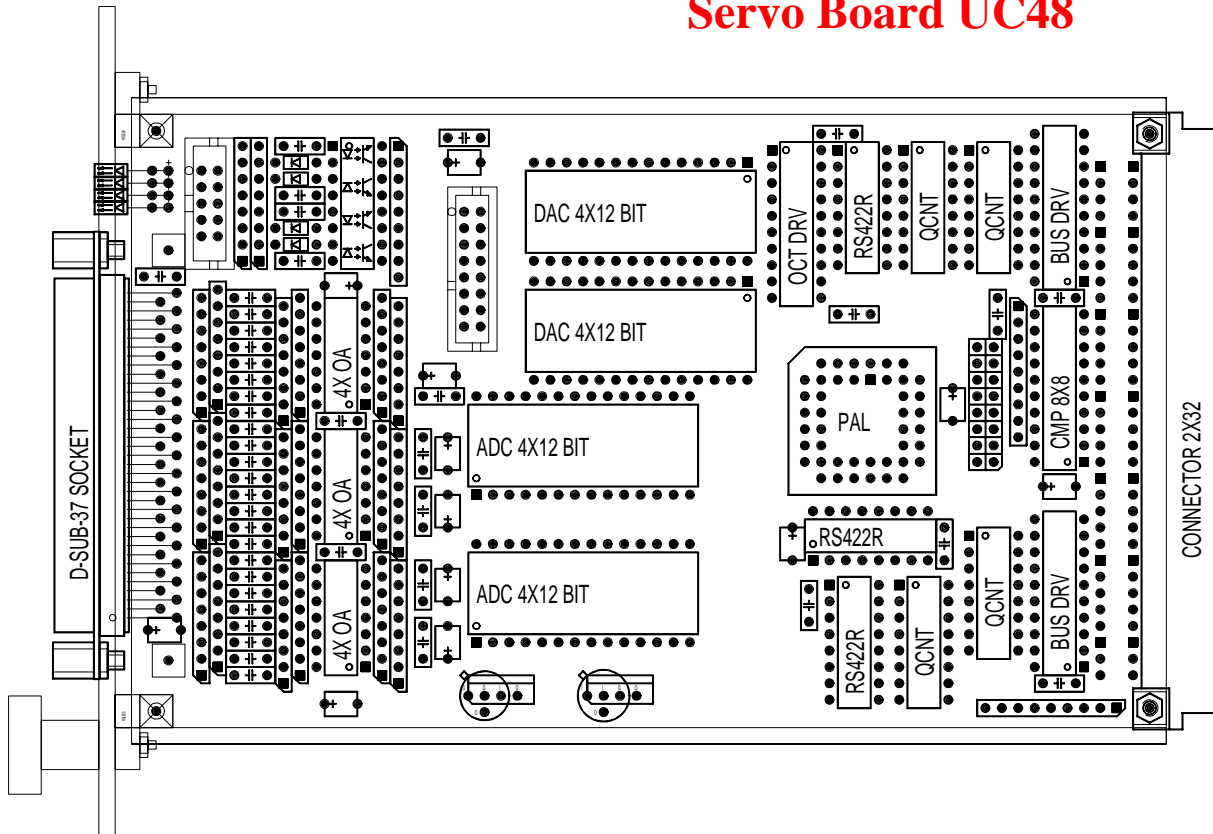


NEW

ROOKH LTD

Servo Board UC48



Features for Servo Board UC48

- Control of step and brushless PM motors
- Euro-board 160 x 100 mm, Eurobus connection with 64 pin connector
- D-Sub-37 connector for four encoder channels.
- Complete control up to 4 servo-axis (Portal X1,X2,Y,Z)
- 4 channels for differential analog inputs sin-cos-ref 1V_{pp} (11 mA optional) for 4 encoders
- Software interpolation for encoder resolution up to 4096 times
- Nanometer-resolutions with standard 20 mkm encoders
- 8 outputs analog 12 Bit 10V bipolar for demand currents or velocities of axes
- 4 opto-coupled inputs 24V for reference switches
- Base address settings per jumper, multiple boards at the same bus possible

Pin assignment for Servo Board UC48

P2 37 pin D-Sub Encoders Female Connector, Front view

			⊙	19	<i>G24</i>	Ground for +24V
End switch axis W	<i>RSW</i>	37	⊙			
			⊙	18	<i>RSZ</i>	End switch axis Z
End switch axis Y	<i>RSY</i>	36	⊙			
			⊙	17	<i>RSX</i>	End switch axis X
+5 V Supply voltage	<i>+5V</i>	35	⊙			
			⊙	16	<i>IWP</i>	Positive ref voltage axis W
Negative ref voltage axis W	<i>IWM</i>	34	⊙			
			⊙	15	<i>BWP</i>	Positive cos voltage axis W
Negative cos voltage axis W	<i>BWM</i>	33	⊙			
			⊙	14	<i>AWP</i>	Positive sin voltage axis W
Negative sin voltage axis W	<i>AWM</i>	32	⊙			
			⊙	13	<i>GND</i>	Ground
+5 V Supply voltage	<i>+5V</i>	31	⊙			
			⊙	12	<i>IZP</i>	Positive ref voltage axis Z
Negative ref voltage axis Z	<i>IZM</i>	30	⊙			
			⊙	11	<i>BZP</i>	Positive cos voltage axis Z
Negative cos voltage axis Z	<i>BZM</i>	29	⊙			
			⊙	10	<i>AZP</i>	Positive sin voltage axis Z
Negative sin voltage axis Z	<i>AZM</i>	28	⊙			
			⊙	09	<i>GND</i>	Ground
+5 V Supply voltage	<i>+5V</i>	27	⊙			
			⊙	08	<i>IYP</i>	Positive ref voltage axis Y
Negative ref voltage axis Y	<i>IYM</i>	26	⊙			
			⊙	07	<i>BYP</i>	Positive cos voltage axis Y
Negative cos voltage axis Y	<i>BYM</i>	25	⊙			
			⊙	06	<i>AYP</i>	Positive sin voltage axis Y
Negative sin voltage axis Y	<i>AYM</i>	24	⊙			
			⊙	05	<i>GND</i>	Ground
+5 V Supply voltage	<i>+5V</i>	23	⊙			
			⊙	04	<i>IXP</i>	Positive ref voltage axis X
Negative ref voltage axis X	<i>IXM</i>	22	⊙			
			⊙	03	<i>BXP</i>	Positive cos voltage axis X
Negative cos voltage axis X	<i>BXM</i>	21	⊙			
			⊙	02	<i>AXP</i>	Positive sin voltage axis X
Negative sin voltage axis X	<i>AXM</i>	20	⊙			
			⊙	01	<i>GND</i>	Ground

All sin, cos, ref voltages are differential 1V_{pp} (point to point) voltages of encoder with return GND. Voltage range of sin, cos, ref differential inputs is 2.5V +/- 0.5V (from 2 to 3V). End switch voltages are +24V opto-coupled voltages with return G24, input resistance is 2 Kohm. End switch voltage range is from 20 to 30V DC, current from 10 to 15 mA. Inductive proximity sensors (opener) are recommended as end switches. Use twisted pair screened cable, screen connection to connectors case

P4 26 pin DAC Output T&B-26 Male Connector, Front view

+5V internal supply voltage	+5V	01	⊙	⊙	02	GND	Ground
+5V internal supply voltage	+5V	03	⊙	⊙	04	GND	Ground
+12V internal supply voltage	+12V	05	⊙	⊙	06	GND	Ground
-12V internal supply voltage	-12V	07	⊙	⊙	08	GND	Ground
Not connected	NC	09	⊙	⊙	10	GND	Ground
DAC output phase B axis W	VWB	11	⊙	⊙	12	GND	Ground
DAC output phase A axis W	VWA	13	⊙	⊙	14	GND	Ground
DAC output phase B axis Z	VZB	15	⊙	⊙	16	GND	Ground
DAC output phase A axis Z	VZA	17	⊙	⊙	18	GND	Ground
DAC output phase B axis Y	VYB	19	⊙	⊙	20	GND	Ground
DAC output phase A axis Y	VYA	21	⊙	⊙	22	GND	Ground
DAC output phase B axis X	VXB	23	⊙	⊙	24	GND	Ground
DAC output phase A axis X	VXA	25	⊙	⊙	26	GND	Ground

All DACs outputs are 10V bipolar voltages with resolution 12 bits with return GND and power-on reset to bipolar zero. Output current is 5 mA max, load resistance 2 KOhm min.

Connector is optimized for ribbon cable montage

Pinout is compatible with Power Amplifier Cross Board PAT

Base address settings for UC48 Board by Jumper J11-J04

Jumper	J11	J10	J09	J08	J07	J06	J05	J04	Address base
Address bit	A11	A10	A09	A08	A07	A06	A05	A04	
	Off	Off	Off	Off	Off	Off	Off	Off	900FF0
	Off	Off	Off	Off	Off	Off	Off	On	900FE0
	Off	Off	Off	Off	Off	Off	On	Off	900FD0
	Off	Off	Off	Off	Off	On	Off	Off	900FB0
	Off	Off	Off	Off	On	Off	Off	Off	900F70
	Off	Off	Off	On	Off	Off	Off	Off	900EF0
	Off	Off	On	Off	Off	Off	Off	Off	900DF0
	Off	On	Off	Off	Off	Off	Off	Off	900BF0
	On	Off	Off	Off	Off	Off	Off	Off	9007F0

On – Jumper is set (related address bit is 0), Off – Jumper is removed (related address bit is 1)

Default setting is J4-J11 Off Off Off Off Off Off Off Off, Address base 900FF0

Jumper J04 is upper Jumper (marked with S1 on component side of PCB), J11 is downer Jumper

Memory map for Board UC48

Address	R/W	Bits 15-12	Bits 11-8	Bits 7-4	Bits 3-0
900FF0	R	ADC 0,1,2,3			CF3 CF2 CF1 CF0
900FF1	R	ADC 3,4,5,6			DI3 DI2 DI1 DI0
900FF2	R	QC1 LOW		QC0 LOW	
900FF3	R	QC1 HIGH		QC0 HIGH	
900FF4	R	QC3 LOW		QC2 LOW	
900FF5	R	QC3 HIGH		QC2 HIGH	
900FF0	W	DAC0			CF3 CF2 CF1 CF0
900FF1	W	DAC1			Not used
900FF2	W	DAC2			Not used
900FF3	W	DAC3			Not used
900FF4	W	DAC4			Not used
900FF5	W	DAC5			Not used
900FF6		DAC6			Not used
900FF7		DAC7			Not used

Legend:

ADC – Analog to digital converter

DAC - Digital to analog converter

QC – Quadrature counter

CF3-CF0 - calibrate flags bits

DI3-DI0 - digital inputs bits

DSP Timer 0 starts conversion of ADC0-ADC7 and latch QC0-QC3

Conversion end ADC0-ADC7 causes DSP Interrupt request IRQ1

ADC reads must be from software interrupt handler

Four successive read from address 900FF0 read values ADC0-ADC3

Four successive read from address 900FF1 read values ADC4-ADC7

Read high byte from QC first to inhibit change of QC (latch value of QC)

Read low byte from QC refresh QC value